

Article

Demonstration of AlGa_N/Ga_N MISHEMT on Si with Low-Temperature Epitaxy Grown AlN Dielectric Gate

Matthew Whiteside ^{1,*}, Subramaniam Arulkumar ², Yilmaz Dikme ³,
Abhinay Sandupatla ¹ and Geok Ing Ng ^{1,2,*}

¹ School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, Singapore; ABHINAY001@e.ntu.edu.sg

² Temasek Laboratories @ NTU, Nanyang Technological University, Singapore 637553, Singapore; Subramaniam@ntu.edu.sg

³ AIXaTECH GmbH, Thomas-Edison-Str. 5-7, 52499 Baesweiler, Germany; y.dikme@aixatech.com

* Correspondence: whit0001@e.ntu.edu.sg (M.W.); EGING@ntu.edu.sg (G.I.N.)

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Abstract: AlGa_N/Ga_N metal-insulator-semiconductor high-electron-mobility transistors (MISHEMT) with a low-temperature epitaxy (LTE)-grown single crystalline AlN gate dielectric were demonstrated for the first time and the post-gate annealing effects at 400 °C were studied. The as-deposited LTE-AlN MISHEMT showed a maximum drain current (I_{Dmax}) of 708 mA/mm at a gate bias of 4 V and a maximum extrinsic transconductance (g_{mmax}) of 129 mS/mm. The 400 °C annealed MISHEMT exhibited an increase of 15% in g_{mmax} , an order of magnitude reduction in reverse gate leakage and about a 3% suppression of drain current (I_D) collapse. The increase of g_{mmax} by post-gate annealing is consistent with the increase of 2DEG mobility. The suppression of I_D collapse and the reduction of gate leakage current is attributed to the reduction of interface state density ($5.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) between the AlN/GaN interface after post-gate annealing at 400 °C. This study demonstrates that LTE grown AlN is a promising alternate material as gate dielectric for GaN-based MISHEMT application.

Keywords: LTE; AlN; AlGa_N/Ga_N; interface state density; conductance-frequency; MISHEMT

1. Introduction

AlGa_N/Ga_N based high-electron-mobility transistors (HEMTs) have demonstrated excellent high-frequency and high-power performance owing to their excellent material properties, such as large breakdown field, wide band gap and high electron mobility [1–4]. However, two of the major limiting factors that conventional Ga_N HEMTs with Schottky metal gates suffer from are a high gate leakage current, and current collapse [5]. The high gate-leakage occurs due to the Schottky metal contact, while current collapse is caused by charge trapping at the surface states present on the AlGa_N surface. To solve these issues, various materials such as Al₂O₃ [6,7], HfO₂ [8] or ZrO₂ [9] have been used as both a passivation layer and gate dielectrics. Among non-oxide insulators, AlN is an attractive high-k dielectric material for III–N metal-insulator-semiconductor high-electron-mobility transistors (MISHEMTs) due to its high breakdown field and high dielectric constant [10,11]. In addition, AlN is of interest due to its high thermal conductivity ($200 \text{ WK}^{-1} \text{ m}^{-1}$), which makes it suitable for use as a passivation layer to suppress the self-heating [12]. AlN has also been reported to help reduce current collapse [13]. There are two main methods used for the deposition of AlN namely metal-organic chemical vapor deposition [14] (MOCVD) and plasma-enhanced atomic layer deposition [15,16] (PEALD). However, the growth temperature of MOCVD (>600 °C) is not desirable for the fabrication of AlGa_N/Ga_N HEMTs. Furthermore, using a lower growth temperature also has the advantage of preventing tensile strain-induced cracking of AlN layer in AlN based MIS-HEMTs [17,18]. PEALD is

a different approach to grow AlN films which can form a better interface with GaN at 350 °C but with a low deposition rate [19]. Recently, Dikme et al. [20] realized thick single crystalline AlN layers on Si and sapphire substrates at 200 °C using a novel technique called low-temperature epitaxy (LTE). In this technique, AlN is deposited as a combination of physical vapor deposition (PVD) and chemical vapor deposition (CVD). LTE also allows for thick (~1 µm) crystalline films to be grown at low-temperatures which is compatible with III-V device processing. We have recently reported the properties of interface states for AlGaIn/GaN metal-insulator-semiconductor diodes (MIS-diodes) using the LTE grown AlN [21,22]. So far, no reports have discussed the AlGaIn/GaN MISHEMTs with LTE-AlN and its post-gate annealing effects. In this paper, we report AlGaIn/GaN MISHEMTs on Si substrate with LTE grown AlN through DC, pulsed I-V and interface trap characterization and analysis.

2. Materials and Methods

The AlGaIn/GaN HEMT structure on Si (111) substrate was grown by MOCVD. It consists of i-GaN (2 nm) cap layer, i-Al_{0.27}Ga_{0.73}N (18 nm) barrier layer, i-GaN (800 nm) buffer layer and transition layer (1400 nm). The resistivity of the Si substrate is >10,000 Ω.cm. Hall samples of (i) as-grown HEMT without LTE-AlN, (ii) HEMT with as-deposited ~8 nm LTE-AlN, (iii) HEMT with LTE-AlN annealed at 400 °C and (iv) HEMT with LTE-AlN annealed at 450 °C were prepared and their results at room temperature are summarized in Table 1. The MISHEMT fabrication process started with mesa isolation by reactive ion etching (RIE) using a Cl₂/BCl₃ mixture. The ohmic contacts consisting of Ti/Al/Ni/Au (20/120/40/50 nm) was deposited followed by rapid thermal annealing at 825 °C for 30 s in an N₂ atmosphere. Transmission line measurements showed a contact resistance of 0.4 Ω mm. Next, the gate dielectric layer using single crystalline AlN with a thickness of ~8 nm was deposited at 200 °C by LTE. The thickness of the deposited LTE-AlN has previously been confirmed by TEM and is reported elsewhere [22]. The novel growth method combines physical vapor deposition (PVD) and chemical vapor deposition (CVD). The Al source is solid Al with a purity of 5N, while the N source is N₂ gas with purity of 5N8. The N was activated by a linear ion gun close to the sample surface and the Al was sputtered in a way that its beam overlaps with the ion gun beam. The substrate temperature was in the range of 200–225 °C and the deposition pressure was in the upper 10⁻³ mbar range with a total power density of around 5–7 W/cm². Before the deposition, the sample was cleaned with a weak Ar/H₂ plasma to remove the native oxide. More details of the growth conditions can be found in the paper by Dikme et al. [20,21].

Table 1. 2DEG properties of AlGaIn/GaN with and without AlN and its post deposition annealing at 400 °C and 450 °C for 300 s in N₂.

2DEG Parameters	AlGaIn/GaN HEMT Structure			
	Without LTE-AlN [22]	As-dep. [22]	With LTE-AlN	
			Annealing Temperature °C	
			400	450
Sheet Resistance (Ω/□)	591	523	520	512
Hall Mobility (cm ² V ⁻¹ s ⁻¹)	1440	1210	1330	1360
Sheet Carrier Concentration (×10 ¹² cm ⁻²)	7.35	9.89	9.02	8.76

The gate metal stack Ni/Au (50/200 nm) was subsequently formed on the LTE grown AlN by electron beam evaporation. Finally, metal thickening (Ti/Au 10/400 nm) was also performed after AlN etching by Cl₂/BCl₃/Ar (40/20/10 sccm) plasma. The inset of Figure 1a shows the cross-sectional schematic diagram of the fabricated MISHEMTs with LTE-grown AlN. For this study, we have used device dimensions of L_g/L_{sg}/L_{gd}/W_g = 2/2/2/(2 × 100) µm. To study the post-gate annealing effects a MISHEMT sample with ~8 nm of LTE-AlN were annealed at 400 °C in a N₂ atmosphere using rapid thermal annealing process. A post-gate annealing temperature of 400 °C was chosen as there

was minimal changes to the Hall parameters after post deposition annealing at 450 °C (see Table 1). A lower temperature is also beneficial, as higher temperatures have previously been shown to cause degradation of Ni/Au gates [23,24].

3. Results and Discussion

Figure 1 shows (a) the capacitance-voltage (C-V) and (b) gate leakage current (I_{gleak}) characteristics of Schottky diode (MS-diode), LTE-AlN MIS-diode with and without post-gate annealing. At zero-bias, the capacitance density of 373 nF/cm² and 302 nF/cm² for 200 μm diameter conventional Schottky diode and MIS-diode were obtained, respectively. After annealing, there is no significant change in capacitance density at 0 V. With reference to Schottky diode, the LTE-AlN MIS-diode exhibited 2 orders of magnitude lower I_{gleak} at −20 V (Figure 1b). After post-gate annealing at 400 °C, MIS-diodes exhibited about an order of magnitude further reduction in I_{gleak} . The improvement in I_{gleak} is attributed to the improvement of interface properties of LTE-AlN on GaN/AlGaN after the 400 °C annealing.

Figure 2 shows (a) current–voltage ($I_{\text{ds}}-V_{\text{ds}}$) and (b) transfer characteristics of LTE-AlN/AlGaN/GaN MISHEMTs without and with post-gate annealing at 400 °C. The as-deposited AlN MISHEMT showed a maximum drain current (I_{Dmax}) of 708 mA/mm at a gate bias of 4 V and a maximum extrinsic transconductance (g_{mmax}) of 129 mS/mm. After annealing, MISHEMT exhibited I_{Dmax} of 684 mA/mm at a gate bias of 4 V and g_{mmax} of 148 mS/mm. The decrease in I_{Dmax} after annealing originates from a change in two-dimensional electron gas (2DEG) carrier concentration (n_s), as $I_{\text{D}} \propto n_s$. As shown in Table 1, after annealing at 400 °C, n_s was found to decrease by 9% (from $9.89 \times 10^{12} \text{ cm}^{-2}$ to $9.02 \times 10^{12} \text{ cm}^{-2}$) which results in the 9% reduction in I_{Dmax} . Similarly, the 15% improvement of g_{mmax} after post-gate annealing is attributed to an increase in electron mobility as well as a reduction of interface states [25]. This is attributed to a reduction in Coulomb scattering from the dielectric layer near the AlGaN/GaN interface [26]. The enhanced mobility was confirmed by Hall measurements, which shows an ~10% improvement (from $1210 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ to $1330 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) in 2DEG Hall mobility (μ_n), as seen in Table 1. From the Figure 2b, it is clear that AlN MISHEMT exhibited an order of magnitude improvement in the device $I_{\text{ON}}/I_{\text{OFF}}$ ratio after the post-gate annealing at 400 °C, which is due to the reduction of drain current at OFF-state. This is possibly caused by a reduction on traps at the AlN/GaN interface reducing the available leakage current conduction paths. The threshold voltages (V_{th}) of the devices were measured at −3.95 V and −3.8 V for as-deposited MISHET and post-gate annealed MISHEMT at 400 °C, respectively. V_{th} can be expressed as

$$V_{\text{th}} = V_{\text{th0}} - \frac{Q_{\text{it}}}{C_{\text{AlN}}} \quad (1)$$

where V_{th0} is the threshold voltages without any interface states, Q_{it} is the interface-trapped charge density and C_{AlN} is the capacitance of the AlN layer. After annealing at 400 °C there is a minimal positive shift in threshold voltage which could be caused by a slight reduction of interface traps at LTE-AlN/GaN interface. This is verified by the frequency-dependent conductance measurements discussed in the later section. A similar occurrence was also reported after post-gate annealing by Zhou et al. for Al₂O₃ and Shih et al. for HfO₂ [8,25]. In these cases, it was postulated that the positive V_{th} shift was caused by a reduction in positively charged traps and interface traps or positive fixed/mobile charges, and was confirmed by a reduction in calculated interface states after annealing. A benchmarking table between these devices and those published elsewhere can be seen in Table 2 [15,27–29].

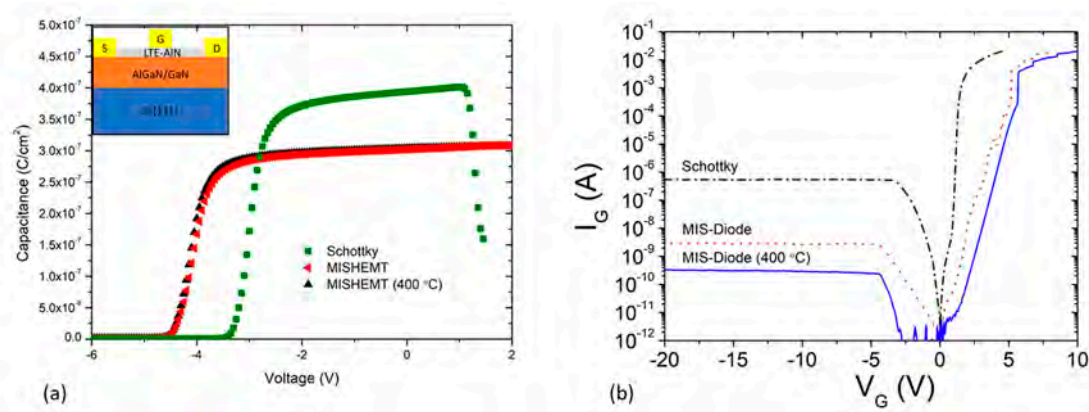


Figure 1. (a) C-V characteristics and (b) two terminal $I_{g\text{leak}}-V_g$ (200 μm diameter diodes) characteristics of Ni/AlGaIn/GaN Schottky diode, as-deposited LTE-AlN/AlGaIn/GaN metal-insulator-semiconductor diode [22] and post-gate annealed MIS-diode at 400 °C. Inset: Schematic cross-sectional diagram of fabricated AlGaIn/GaN MISHEMTs with LTE grown AlN on Si substrate.

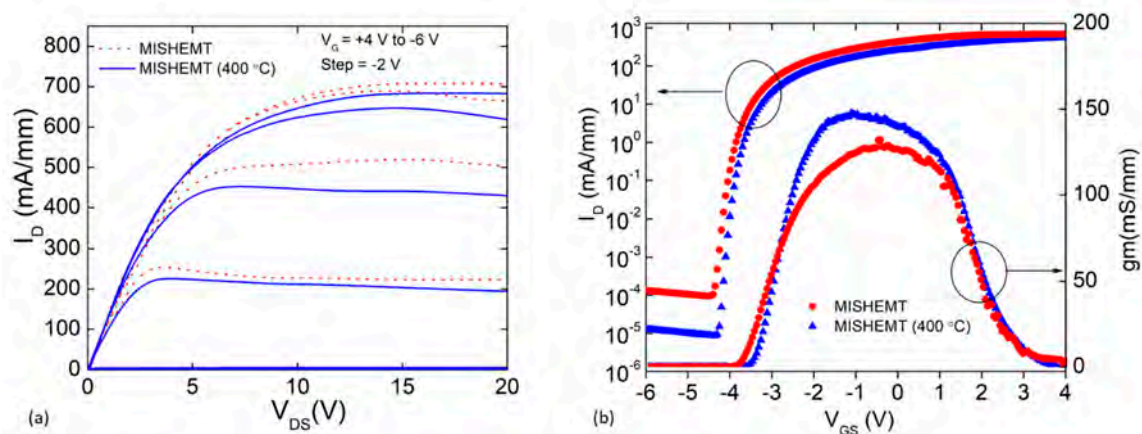


Figure 2. (a) DC $I_{DS}-V_{DS}$ and (b) transfer characteristics of as-deposited LTE-AlN/AlGaIn/GaN MISHEMT and post-gate annealed MISHEMT at 400 °C.

Table 2. A benchmarking table for MISHEMT on AlGaIn/GaN using AlN as a gate dielectric layer.

Reference	Thickness (nm)	Substrate	Deposition Method	Device Dimensions L_g/W_g (μm)	$I_{d\text{max}}$ (mA/mm)	$g_{m\text{max}}$ (mS/mm)	On/Off Ratio (Orders of Magnitude)
[15]	10.6	Si	ALD	2.5/60	563 @ 5V	87	~5
[27]	10	Sapphire	ALD	1/200	600 @ 4V	127	~9
[28]	20	Sapphire	PEALD	0.5/50	~1050 @ 2 V	289	~3
[29]	8	SiC	Reactive Sputtering	0.4/200	~1250 @ 2 V	260	~3
This work	8	Si	LTE	2/(2 × 100)	684 @ 4V	148	~8

Figure 3 shows pulsed I_D-V_D characteristics of (a) as-deposited MISHEMTs with LTE-AlN and (b) MISHEMTs with post-gate annealing at 400 °C. The devices were subjected to the pulse width/period of 100 μs /10ms and quiescent biases of $(V_{gs0}, V_{ds0}) = (0, 0)$ and $(-6, 20)$ V was used for the pulsed I-V measurements. The as-deposited LTE-AlN MISHEMT exhibited a $I_D/I_{D\text{max}}$ ratio of 0.91 for both quiescent biases $(V_{gs0}, V_{ds0}) = (0, 0)$ and $(-6, 20)$. This indicates that the devices exhibited around 9% drain current (I_D) collapse. After annealing at 400 °C, the $I_D/I_{D\text{max}}$ ratio of MISHEMT increases to 0.94. Therefore, about 3% I_D collapse was suppressed after post-gate annealing at 400 °C. The improvement in current collapse in 400 °C annealed MISHEMT is attributed to the reduction of interface states at the AlN/GaN interface.

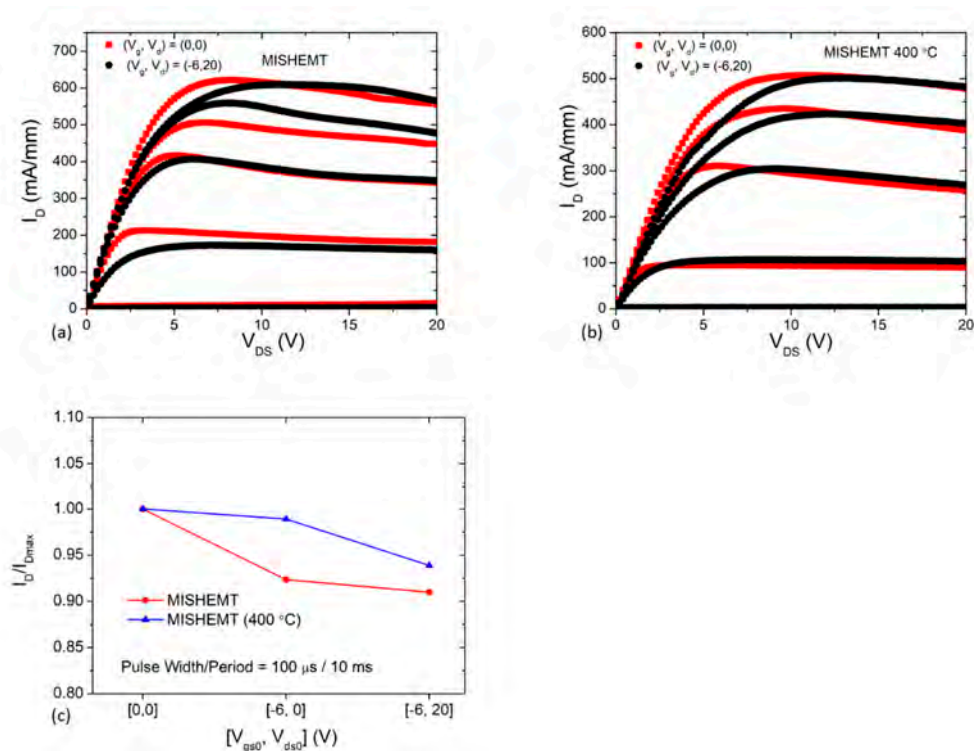


Figure 3. Pulsed I_{DS} - V_{DS} characteristics at quiescent bias points of $(V_{gs0}, V_{ds0}) = (0, 0), (-6, 20)$ for (a) LTE-AlN MISHEMTs, (b) 400 °C annealed MISHEMTs and (c) normalized I_D with I_{Dmax} for as-deposited LTE-AlN/AlGaIn/GaN MISHEMT and annealed MISHEMT at 400 °C vs. the quiescent bias points $(V_{gs0}, V_{ds0}) = (0, 0), (-6, 0), (-6, 20)$ V.

In order to quantify the amount of interface states at the LTE-AlN/GaN interfaces, frequency-dependent conductance measurements were performed at selected biases to estimate the density of interface states (D_{it}) and trap time constant (τ_{it}). The frequency was varied from 1 kHz to 5 MHz over a wide range of gate voltages (V_g). Figure 4a shows the typical G_p/ω versus ω graph of LTE-AlN MISHEMT with post-gate annealed at 400 °C measured at different V_g values between -4.1 V to -3.5 V. The D_{it} calculations were performed using the conductance-frequency method, which is widely used for interface calculations [21,30,31]. The two peak regions in the G_p/ω plots correspondingly indicate the presence of both low frequency (slow traps) and high frequency (fast traps). The exhibited fast traps are associated interface traps of the AlGaIn/GaN hetero-interface [15,32], while the observed slow traps are associated with the AlN/GaN interface. The estimated D_{it} is shown in Figure 4b for the as-deposited LTE-AlN MIS-diode, as well as the MIS-diodes with post-gate annealing at 400 °C. The minimum D_{it} were estimated as $7.6 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ and $5.0 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ for the as-deposited MIS-diode and MIS-diode with post-gate annealing at 400 °C, respectively. With reference to as-deposited MIS-diode, a reduction of D_{it} (24%) has been observed in the MIS-diode after post-gate annealing at 400 °C. This reduction of interface traps can be associated with the suppression of I_D collapse. Annealing at 400 °C helps to reduce the slow deep level traps thus reducing the remote Coulomb scattering from the AlN layer and improving the mobility.

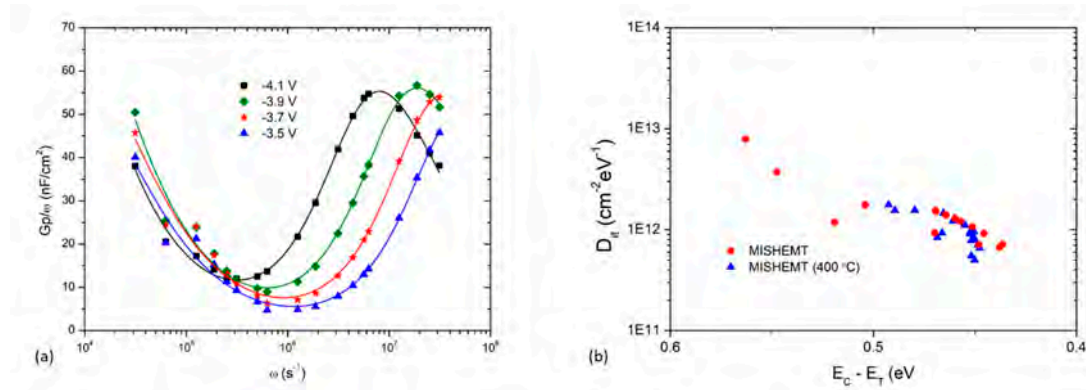


Figure 4. (a) G_p/ω versus radial frequency plot for different gate voltages of post-gate annealed LTE-AlN MIS-diode at 400 °C (solid lines are fitting curves). (b) Distribution of interface state density as a function of the gate voltage of as-deposited LTE-AlN MIS-diodes [22] and post-gate annealed MIS-diodes at 400 °C.

4. Conclusions

In summary, AlGaIn/GaN MISHEMTs on Si has been demonstrated for the first time with LTE grown AlN as a dielectric layer. The influence of post-gate annealing at 400 °C was also studied using DC, pulsed I-V and interface state characteristics. After the LTE-AlN deposition the LTE-AlN MISHEMT showed a maximum drain current (I_{Dmax}) of 708 mA/mm at a gate bias of 4 V and a maximum extrinsic transconductance (g_{mmax}) of 129 mS/mm. By employing a post-gate annealing scheme at 400 °C in an N_2 atmosphere there was about a 15% of increase in g_{mmax} and an order of magnitude reduction of gate leakage. About a 3% improvement of I_D collapse suppression was also observed after post-gate annealing at 400 °C. The reduction of I_{gleak} and I_D collapse could be due to the reduction of interface state density of about 25%. This study indicates that the optimized post-gate annealing, which in our case is at 400 °C, is a viable way to have improved device characteristics in AlGaIn/GaN MISHEMTs with LTE grown AlN.

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